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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/047,809 | 01/15/2002 | Ken Shoemaker | 2207/12020 | 4746 |

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| EXAMINER | |
|---|---|
| VO, LILIAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2127 | |

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/047,809 | SHOEMAKER ET AL. | |
| | Examiner | Art Unit | |
| | Lilian Vo | 2127 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1 – 20 are pending.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 - 7 and 15 – 20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. Referring to **claim 1**, the limitation "wherein said multi-thread scheduler is to determine whether the width of said execution unit" is considered unclear and incomplete. A clarification is required.

B. The following terms lack antecedent basis:

a. "the width", in **claims 1 and 2.**

b. "said multi-threading processor", in **claims 15 and 16**.

c. "the multi-threading processor", in **claims 17 and 19**.

### *Claim Rejections - 35 USC § 101*

4. Claims 9 – 14 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

5. **Claims 9- 14** are directed to method steps, which can be practiced mentally in conjunction with pen and paper, therefore they are directed to non-statutory subject matter. Specifically, as claimed, it is uncertain what performs each of the claimed method steps. Moreover, each of the claimed steps, inter alia, determining, executing, compiling, fetching, decoding, can be practiced mentally in conjunctions with pen and paper. The claimed steps do not define a machine or computer implemented process [see MPEP 2106]. Therefore, the claimed invention is directed to non-statutory subject matter. (The examiner suggests applicant to change "method" to "computer implemented method" in the preamble to overcome the outstanding 35 U.S.C. 101 rejection).

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 9 and 15 rejected under 35 U.S.C. 102(b) as being anticipated by Eggers et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors" (hereinafter Eggers).

8. Regarding **claim 1**, Eggers discloses a multi-threading processor, comprising:

a first instruction fetch unit to receive a first thread (page 14, left column: The fetch unit partitions itself among the threads...) and a second instruction fetch unit to receive a second thread (page 14, left column: The fetch unit partitions itself among the threads.);

an execution unit to execute said first thread and said second thread (pages 13 and 14); and

a multi-thread scheduler coupled to said first instruction fetch unit, said second instruction fetch unit, and said execution unit (page 13, left column, see the description of fig. 1c), wherein said multi-thread scheduler is to determine whether the width of said execution unit (page 13, left column, see description of fig. 1c, page 17, right column, last paragraph).

9. Regarding **claim 9,** Eggers discloses a method for scheduling threads in a multi-threading processor, comprising:

determining whether said multi-threading processor is wide enough to execute a f first thread and a second thread in parallel (page 12, left column, last paragraph – right column, 1st paragraph: SMT processor exploits both types of thread-level and instruction-level parallelism); and

executing said first thread and said second thread in parallel if said multithreading processor is wide enough to execute the first thread and the second thread in parallel (page 12, left column: SMP processor design which meets simultaneous multithreading because it consumes both thread-level and instruction-level parallelism. Page 13, left

column, fig. 1c description: if multiple threads each have low instruction-level parallelism, they can be executed together to compensate).

10. **Claim 15** is rejected on the same ground as stated in claim 9 above.

### *Claim Rejections - 35 USC § 103*

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eggers et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors".

13. Regarding **claim 2**, Eggers discloses a SMT system with a processor design to exploit all types of parallelism including consuming both thread-level and instruction-level parallelism and that SMT processors use resources more efficiently (page 12, left column, 2nd paragraph – right column, 1st paragraph). Eggers also discloses that SMT uses instruction-level and thread-level parallelism to substantially increase effective processor utilization and to accelerate both multiprogramming and parallel workloads (page 17, right column, last paragraph). It would have been obvious to one of an ordinary skill in the art, to recognize that the multi-thread scheduler unit in Eggers' system determines whether the execution unit is to execute the first thread and the second

thread in parallel depending on the width of the execution unit for effectively utilizing the processor and accelerating both multiprogramming and parallel workloads.

14. Claims 3 – 8, 10 – 14 and 16 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eggers et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors", as applied to claims 1, 9 and 15 above, in view of Applicant's admitted prior art (hereinafter AAPA).

15. Regarding **claim 3**, Eggers discloses a SMT's system that can perform instruction-level parallelism (page 12, left column, last paragraph). It would have been obvious to one of an ordinary skill in the art, at the time the invention was made to consider Egger's system an in-order processor because if one thread has high instruction-level parallelism, that parallelism can be satisfied (page 13, left column, 6$^{th}$ paragraph). Furthermore, AAPA discloses that an in-order processor is a well-known architecture in the art (specification page 3, lines 10 – 15).

16. Regarding **claim 4**, as modified Eggers discloses the execution unit executes the first thread and the second thread in parallel (Eggers: page 13, left column, fig. 1c description: if multiple threads each have low instruction-level parallelism, they can be executed together to compensate).

17. Regarding **claim 5**, as modified Eggers discloses the execution unit executes the first thread and the second thread in series (Eggers: page 13, left column, fig. 1c

description: if one thread has high instruction-level parallelism, that parallelism can be satisfied).

18. Regarding **claim 6**, as modified Eggers discloses the first thread and the second thread are compiled to have instruction level parallelism (Eggers: page 12, left column, last paragraph).

19. Regarding **claim 7**, as modified Eggers discloses a multi-threading processor comprising:

a first instruction decode unit coupled between the first instruction fetch unit and the multi-thread scheduler (Eggers: page 14, right column, 1st paragraph: the decoder for the first thread instructions); and

a second instruction decode unit coupled between the second instruction fetch unit and the multi-thread scheduler (Eggers: page 14, right column, 1st paragraph: the decoder for the second thread instructions).

20. Regarding **claim 8,** as modified Eggers discloses the execution unit executes only two threads in parallel (Eggers: page 14, left column, 5th - right column, 2nd paragraph: on each cycle, it selects two different threads).

21. Regarding **claim 10,** as modified Eggers discloses a method for scheduling threads comprising executing the first thread and the second thread in series if said multi-

threading processor is not wide enough (Eggers: page 13, left column, fig. 1c description).

22. **Claims 11 – 14 and 16 - 20** are rejected on the same ground as stated in claims 3, 6 – 8 and 10 above.

***Conclusion***

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Levy et al. (US 2001/0004755) discloses a system for freeing renaming registers on processors with multiple fetch units.

Shiell et al. (US 5,913,049) discloses a system including multi-stream pipeline unit.

Rivers et al. (US 2002/0174319) discloses a method and apparatus for reducing logic activity in a microprocessor.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2127

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March 4, 2005

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